

## **Salah Harb, Ph.D.**

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### **EDUCATION**

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- ❖ **Florida Institute of Technology — Melbourne, FL, USA**
  - Research Fellow at Computational Mathematics and Data Science Center, Jan 2026
  - Project Title: An AI-Assisted Cloud-Native Repository for Medical Imaging Data Analysis
  
- ❖ **Lawrence Berkeley National Laboratory — Berkeley, CA, USA**
  - Postdoctoral Scholar at Accelerator Technology & Applied Physics (ATAP) Division, Jan 2024
  - Project Title: A Versatile, High Resolution Distributed Fiber-optic Sensing Platform
  - Funded by Department of Energy (DOE)
  
- ❖ **Concordia University — Montreal, Canada**
  - Ph.D. in Electrical and Computer Engineering, Graduated, November 2023
  - Thesis Title: Development of a Secure Lossless Model for Image Steganography and its Hardware Realization for Real-Time Applications
  - Advisors: Prof. M. Omair Ahmad and Prof. M.N.S. Swamy
  
- ❖ **Jordan University of Science and Technology (JUST) — Irbid, Jordan**
  - M.Sc. in Computer Engineering, Graduated, April 2014
  - Thesis Title: FPGA Based Embedded System Implementation of AES Algorithm
  - Advisor: Prof. Khaldoun Mhaidat
  
- ❖ **Jordan University of Science and Technology (JUST) — Irbid, Jordan**
  - B.Sc. in Computer Engineering, Graduated, June 2011

### **RESEARCH INTERESTS**

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- ❖ **Research Interests & Technical Expertise:**
  - Hardware Acceleration & Security
  - Photonics & Sensing
  - Machine Learning & AI
  - Distributed & High-Performance Computing
  - Signal Processing & FFT
  - Steganography & Image Processing
  - Networked Systems
  
- ❖ **Particular subjects include:**
  - Optical Frequency Domain Reflectometry (OFDR) and Fiber Optics
  - Field Programmable Gate Arrays (FPGAs) Prototyping
  - Symmetric & Asymmetric Encryption /Decryption Algorithms
  - Image Steganographic Schemes
  - Embedded System Design in Soft/Hard processors (MicroBlaze/PowerPC)
  - Zynq-7000 SoC, RFSoc 4x2 and Pynq Platforms
  - High-Level Synthesis (HLS) Translation
  - Arithmetic Circuit Design
  - ADC, DAC, I/O, AXI and DMA Interfacing
  - Intellectual Property (IP) Cores

- FPGA-Based Memory Management
- Wireless Sensors Networks Protocols and M2M 6G Networks
- Neural Networks Development

## SKILLS

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- ❖ **Operating Systems:** UNIX based systems (Linux) and Windows.
- ❖ **Programming Languages:** C, C++, Python, Java, C#, SQL, JavaScript, HTML, PHP, ASP.Net, Hardware Description Language (Verilog, VHDL & SystemVerilog), Bash, TCL.
- ❖ **Cloud and Data Platforms:** AWS, Amazon S3, Databricks.
- ❖ **Tools:** Microsoft Visual Studio, Eclipse, NetBeans, Xilinx ISE, Xilinx ISim, Xilinx EDK (XPS), Xilinx SDK, Vivado Suite, Xilinx Vitis HLS, ModelSim, SynaptiCAD, Jupyter Notebooks, Jira.
- ❖ **Special Skills:** Low power & high-speed FPGA-based implementations, recursive and pipelining architectures.

## EXPERIENCE

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### ❖ Field Experience:

- **Florida Tech: Research Fellow at Computational Mathematics and Data Science Center—**  
*Melbourne, FL, USA. January 2026 – Present*
  - Designing and implementing an AI-assisted, cloud-native medical imaging data repository, integrating AWS S3 for scalable storage and Databricks for distributed, analysis-ready data processing and discovery.
  - Developing AI-driven natural language dataset discovery and extensible analytics workflows, supporting metadata-driven analysis, built-in applications, and user-defined containerized pipelines with secure governance and reproducible deployment.
- **LBNL: Accelerator Technology & Applied Physics Division—**  
*Berkeley, CA, USA. January 2024 – January 2026*
  - Designed and implemented a high-resolution Optical Frequency Domain Reflectometry (OFDR) system for distributed fiber-optic sensing.
  - Developed a GPU-accelerated OFDR pipeline (CUDA/CuPy, RTX 4070 Ti) achieving <10 ms latency for real-time compensation and sensing feedback.
  - Implemented and optimized RTL (VHDL, Verilog) modules for signal acquisition, FFT processing, and data resampling.
  - Designed custom FPGA IP cores for high-throughput data transmission, PCIe interfacing, and synchronization with tunable lasers.
  - Integrated Python/Flask multiprocessing pipelines for automated acquisition, cross-correlation, and frequency-shift analysis.
  - Benchmarked and optimized shared-memory multiprocessing pipelines for time-critical OFDR analysis (resampling, FFT, Hilbert transform).
  - Led experiments with fiber-under-test (FUT) setups for temperature/strain sensing; validated system accuracy with localized and distributed heating experiments.
  - Developed FPGA designs on the AMD Xilinx RFSoc 4x2 platform, leveraging DDR4 memory, DMA engines, and integrated ADC/DAC interfaces for real-time data acquisition.
  - Configured and utilized QSFP28 high-speed transceivers for scalable multi-gigabit data offloading and system integration.

- **MDA: Satellite and Robotic systems**— *Montreal, Canada. October 2022 – March 2023*
  - Implemented RTL (VHDL/Verilog) modules for satellite communication and control systems, focusing on payload control unit integration for the CanadaARM robotic system.
  - Designed and executed comprehensive RTL test benches to verify timing, functionality, and reliability of mission-critical modules under aerospace-grade constraints.
  - Integrated and debugged FPGA-based RTL designs in embedded avionics environments with strict performance, redundancy, and fault-tolerance requirements.

❖ **Academic Experience:**

- **Advanced encryption standard (AES)**— *PhD work, January 2022 - March 2022*
  - Designed and implemented a reconfigurable high-speed core suitable for large-scale embedded systems and their applications.
  - Developed and implemented a prototype of a real-time application for encrypting plaintexts written in SD memory using ZedBoard Zynq-7000 SoC development board.
- **Image steganography**— *PhD work, February 2020 - December 2023*
  - Proposed a secure lossless model for image steganography using modulus based embedding scheme.
  - Developed and implemented a prototype of a real-time application for enhancing sizes of digital images using ZedBoard Zynq-7000 SoC development board.
- **Elliptic curve (EC) cryptosystem**— *PhD work, March 2020 - May 2020*
  - Designed a reconfigurable implementation of a high-speed core using efficient projective coordinate system.
- **Paillier public key cryptosystem**— *PhD work, January 2020 - March 2020*
  - Designed a reconfigurable implementation of a separable Image steganographic scheme.
- **Image steganography**— *PhD work, November 2019 - January 2020*
  - Developed a high-capacity data hiding scheme using Salt and Pepper (SP) noise.
- **Elliptic curve (EC) cryptosystem**— *Research and development work, December 2018- January 2019*
  - Designed and implemented a reconfigurable, compact core suitable for small embedded applications.
- **Square root computations**— *Research and development work, January 2017 - July 2017*
  - Developed a reconfigurable, high-speed, and area-efficient core for computations over large finite fields.
- **Solid state drive (SSD)**— *Internship work, July 2016 - September 2017*
  - Enhanced the efficiency of SSDs by improving the time and space of writing operations in memories, leveraging data patterns.
- **Advanced encryption standard (AES)** — *Master work, September 2013 - June 2014*
  - Developed and implemented a reconfigurable, compact core for small-footprint, low-power embedded applications.

- Developed and implemented a prototype of a real-time application for encrypting plaintexts using MicroBlaze softcore processor.
- **Data encryption standard (DES)**— *Bachelor work, July 2010 - June 2011*
  - ❖ Designed and implemented a reconfigurable, compact core optimized for small-footprint, low-power embedded applications.
- ❖ **Teaching Experience:**
  - Teaching Assistant in the Electrical and Computer Engineering Department — Concordia University, Fall and Winter Semesters, 2018-2022.
    - Courses: Digital Systems Design, Computer Architecture and Design, Operating Systems, Advanced Computer Architecture, Computer Organization and Design, Software Engineering.
  - Teaching Assistant in the Electrical and Computer Engineering Department — Jordan University of Science and Technology (JUST), Fall and Winter Semesters, 2012- 2014.
    - Courses: Microprocessor Interfacing, Digital Logic Design, Communication Skills.

## PUBLICATIONS

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### ❖ Journal Papers:

- S. Harb, M. O. Ahmad, and M. N. S. Swamy, “**Hardware-Accelerated Image Steganography for Real-Time Secure Communication on FPGA and Embedded AI Platforms,**” under review by Journal of Information Security and Applications (Elsevier)
- S. Harb, L. Linqing, and G. Huang, “**Real-Time GPU-Accelerated OFDR with an Integrated Auxiliary Interferometer,**” in *IEEE Access*, vol. 14, pp. 12639-12654, Jan. 2026, doi: 10.1109/ACCESS.2026.3656341.
- S. Harb, M. O. Ahmad, and M. N. S. Swamy, “**An Efficient Image Steganographic Scheme for a Real-Time Embedded System and its Hardware Implementation on AMD Xilinx Zynq-7000 APSoC Platform,**” *Journal of Real-Time Image Processing*, vol. 20, p. 46, April 2023.
- S. Harb and M. Jarrah, “**FPGA Implementation of the ECC over GF (2<sup>m</sup>) for Small Embedded Applications,**” *ACM Transactions on Embedded Computing Systems (TECS)*, vol. 18, p. 17, March 2019.
- Zheng Li; Fang Wang, Dan Feng, Yu Hua, Jingning Liu, Wei Tong, Yu Chen, S. Harb. “**Time and Space-Efficient Write Parallelism in PCM by Exploiting Data Patterns,**” in *IEEE Transactions on Computers*, vol. 66, no. 9, pp. 1629-1644, September 2017.
- Bani-Hani, R., S. Harb, Mhaidat, K. “**Very Compact and Efficient 32-Bit AES Core Design using FPGAs for Small-Footprint Low-Power Embedded Applications,**” *Journal of Circuits, Systems, and Computers*, vol. 25, November 2016.
- Badarneh, A., S. Harb, Sawafta, A. “**A Survey on MapReduce Implementations,**” *International Journal of Cloud Applications and Computing (IJCAC)*, IGI Global, vol. 6(1), article (4), pp. 59-87, January 2016.
- Bani-Hani, R., S. Harb, Mhaidat, K. and Taqieddin, E. “**High-Throughput and Area-Efficient FPGA Implementations of Data Encryption Standard (DES),**” *Circuits and Systems*, 5, pp. 45-56, February 2014.

### ❖ Conference Papers:

- S. Harb, T. Daradkeh and Y, Alahmad, “**Cross-Platform Benchmarking of Elliptic Curve Cryptography over GF(2<sup>m</sup>),**” in 2026 17th International Conference on Information and Communication Systems (ICICS), July 2026.
- T. Daradkeh, S. Harb, and Y, Alahmad, “**A Novel Platform Model for IoT Devices M2M Communication in 6G Network,**” in the 2025 International Conference on Computational Science and Computational Intelligence (CSCI'25), December 2025.

- S. Harb, G. Huang, and L. Luo, “**Self-Integrated Auxiliary Interferometer for Nonlinearity Compensation in Optical Frequency Domain Reflectometry**,” in the 29th International Conference on Optical Fiber Sensors (OFS 2025), Proc. of SPIE vol. 13639, May 2025.
- S. Harb, M. O. Ahmad, and M. N. S. Swamy, “**High-Speed Pipelined FPGA Implementation of a Robust Steganographic Scheme for Secure Data Communication Systems**,” in 21st International Conference on Security and Cryptography (SECRYPT 2024), pp 397-406, July 2024.
- S. Harb, M. O. Ahmad, and M. N. S. Swamy, “**A High-Speed FPGA Implementation of AES for Large Scale Embedded Systems and its Applications**,” in 2022 13th International Conference on Information and Communication Systems (ICICS), pp. 59–64, July 2022.
- S. Harb, M. O. Ahmad, and M. N. S. Swamy, “**Design and Hardware Implementation of a Separable Image Steganographic Scheme using Public-Key Cryptosystem**,” in 9th International Conference on Cryptography and Information Security (CRYPIS 2020), vol. 10, pp. 227–240, May 2020.
- A. R. Idrais, S. Harb, M. O. Ahmad and M. N. S. Swamy, "A Novel High-Capacity Data Hiding Algorithm using Salt and Pepper Noise," 2020 11th International Conference on Information and Communication Systems (ICICS, pp. 131-135, April 2020.
- S. Harb, M. O. Ahmad, and M. N. S. Swamy, “**High-performance Pipelined FPGA Implementation of the Elliptic Curve Cryptography over GF (2n)**,” in 2019 International Conference on Security and Cryptography (SECRYPT), vol. 2, pp 15-24, August 2019.
- S. Harb and Moath Jarrah,” **Accelerating Square Root Computations over Large GF (2m)**”, Proceedings of the 14th International Joint Conference on e-Business and Telecommunications (SECRYPT 2017), vol. 4, pp 229 – 236, July 2017.
- Shurman, M.M, Al-Mistarihi, M.F, and S. Harb. “**An Energy-Efficient Coverage Aware Clustering Mechanism for Wireless Sensor Networks**,” in 5th International Conference on Communications, Computers and Applications (MIC-CCA2012) Communications, Computers and Applications (MIC-CCA), Turkey-Istanbul, pp 154 – 158, October 2012.

#### ❖ Chapters in Books

- S. Harb, M. O. Ahmad, and M. N. S. Swamy, “**A Reconfigurable Implementation of Elliptic Curve Cryptography over GF (2n)**,” in 2019 E-Business and Telecommunications, vol. 1247, pp. 87–107, August 2019.

#### FUNDING SUPPORT

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- **Ph.D. – Concordia University, Montreal, Canada**
  - Graduate Student Research (GSR) Fellowship, Concordia University – 2 awards.
  - Research supported for 3 years by the Natural Sciences and Engineering Research Council (NSERC) of Canada and the Regroupement Stratégique en Microélectronique du Québec (ReSMiQ).
- **Postdoctoral Scholar – Lawrence Berkeley National Laboratory, Berkeley, USA**
  - Supported for 2 years by the Laboratory Directed Research and Development (LDRD) Program of Lawrence Berkeley National Laboratory under the U.S. Department of Energy (DOE).
  - Project: Development of high-resolution Optical Frequency Domain Reflectometry (OFDR) system for distributed fiber-optic sensing.

#### AWARDS

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- ❖ **Excellence Graduate Student Research Paper Competition Award, 3rd Place.**
  - March 6th, 2019, Montreal, Canada
- ❖ **Excellence Graduate Student Research Paper Competition Award, 2nd Place.**
  - March 23rd, 2022, Montreal, Canada

## INTERSHIPS AND WORKSHOPS

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- ❖ **Wuhan National Laboratory for Optoelectronics (WNLO)**— Wuhan, China. September 2015 – August 2016,
  - Interned at Huazhong University of Science and Technology (HUST).
  - Attended lectures on Solid State Drivers (SSD) and storage systems.
  - Worked on secure embedded systems and FPGA-based accelerators.
  
- ❖ **SYNOPSYS**— Armenia. June 2013 – June 2013,
  - Trained in Hspice and custom design EDA tools.
  - Created layouts and schematics for digital devices.
  
- ❖ **CISCO Systems**— Jordan. February 2011 – June 2011,
  - Enrolled in CCNA exploration courses covering:
    - Network fundamentals
    - Routing protocols and concepts
    - LAN switching and wireless.